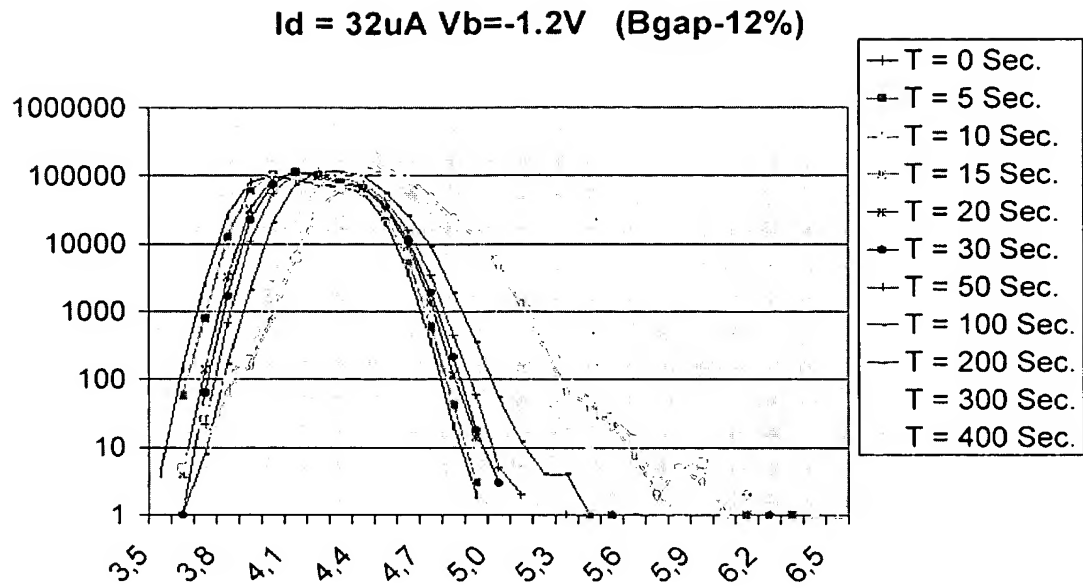
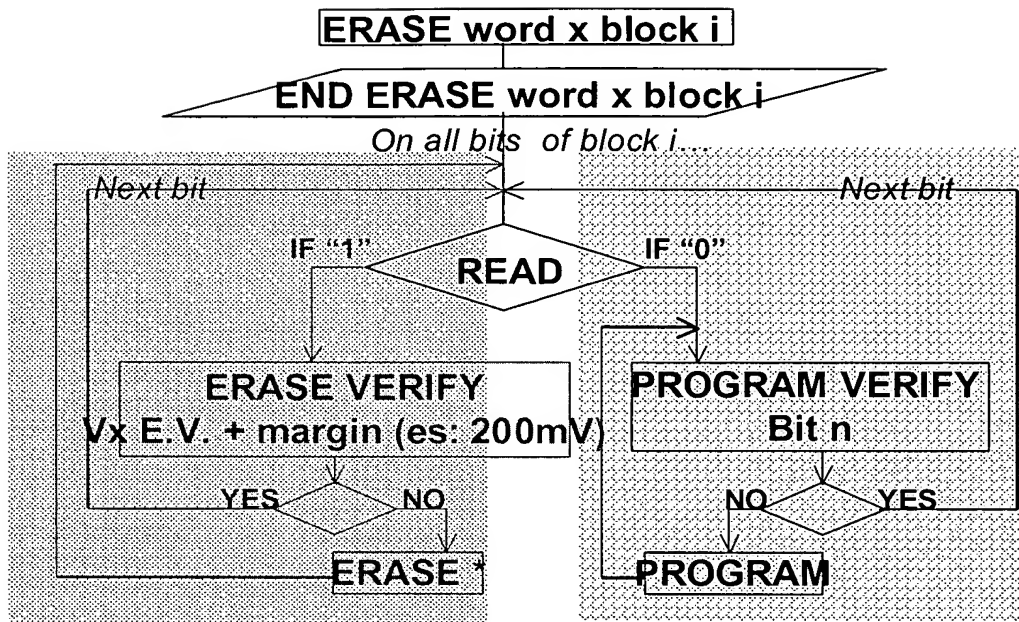
**FIG. 1**

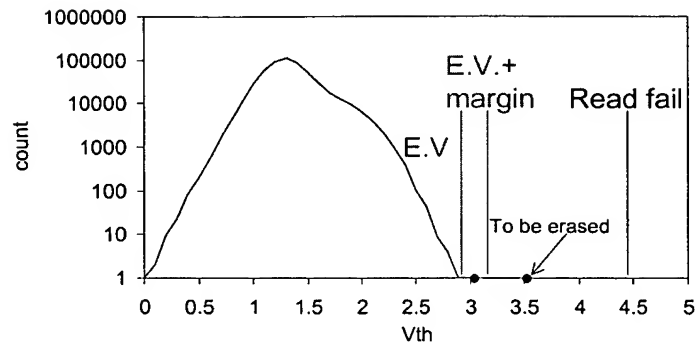
**FIG. 2**



During this cycle the critical "1" bit are identified and erased down to erase verify

During this cycle the critical bit "0" are identified and programmed up to program verify

FIG. 3

**FIG. 4**